Seagate

ST9100A	• • • •	• • • •	• • • •	· • • • •	• • • •
AT Interface Drive	• • • •	• • • •	• • • •		• • •
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Product Manual	• • • •	• • • •			

ST9100A AT Interface Drive Product Manual

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1.0 Specification summary

1.1 Formatted capacity

Guaranteed Mbytes 85.8

Guaranteed sectors 167,552

Bytes per sector 512

1.2 Physical organization

Read/Write heads 2

Discs 1

1.3 Logical organization

Sectors per track (max) 64

Read/Write heads (max) 16

Cylinders (max) Unrestricted

Note. All head, cylinder, and sector geometries are supported subject to the maximums specified and to the following condition:

 $(sectors) \times (heads) \times (cylinders) \le total sectors per drive$

1.4 Default logical geometry

Sectors per track 16

Read/Write heads 14

Cylinders 748

1.5 Functional specifications

Interface AT

Recording method RLL (1,7)
Recording density (BPI) 58,200
Flux density (FCI) 43,760
Track density (TPI) 2,650

Spindle speed (RPM) $3,545 \pm 0.5\%$

Internal data transfer rate up to 22.4 Mbits/sec (6 zones)—ZBR

I/O data transfer rate up to 4 Mbytes/sec

Interleave 1:1

Buffer 120 Kbytes

1.6 Physical dimensions

 Height (max)
 0.504 inches (12.80 mm)

 Width (max)
 2.760 inches (70.10 mm)

 Depth (max)
 4.001 inches (101.85 mm)

Weight (max) 4.8 oz (0.136 Kg)

1.7 Seek time

Seek time is a true statistical average (at least 5,000 measurements) of seek time, less controller overhead. All measurements are made with nominal power at sea level and 25°C ambient temperature. Track-to-track seek time is an average of all possible single-track seeks in both directions. Average seek time is measured by executing seek commands between random sector addresses. Full-stroke seek time is one-half the time needed to seek from the first data sector to the maximum data sector and back to the first sector. Host overhead varies between systems and cannot be specified.

Track-to-track

typical avg. (msec) 5 maximum avg. (msec) 7

Average

typical avg. (msec) 16 maximum avg. (msec) 19

Full-stroke

typical avg. (msec) 26 maximum avg. (msec) 28 Average latency (msec) 8.46

1.8 Spinup times (typical)

Spinup time from Power-on to Ready is 10 seconds (typical). Spinup time from Standby to Ready is 3 seconds (typical).

1.9 Reliability

Nonrecoverable read errors 1 per 10¹³ bits read

Mean time between failures 300,000 power-on hours

(nominal power, at sea level, 25°C ambient temperature)

Preventative maintenance None required

Mean time to repair 10 minutes

Service life 5 years

1.10 Environment

1.10.1 Acoustics

30 dBA maximum (sound pressure) in Idle mode, at 1 meter.

1.10.2 Ambient temperature

Operating 5° to 55°C (41° to 131°F)

Nonoperating -40° to 70°C (-40° to 158°F)

1.10.3 Temperature gradient

Operating 30°C/hr max (54°F/hr), without condensation Nonoperating 30°C/hr max (54°F/hr), without condensation

1.10.4 Relative humidity

Operating 8% to 80% noncondensing;

Max. wet bulb temperature: 40°C (78.8°F)

Nonoperating 8% to 90% noncondensing

Max. wet bulb temperature: 56°C (132°F)

1.10.5 Altitude

Operating -1,000 ft to 10,000 ft (-304.8 m to 3,048 m)

Nonoperating -1,000 ft to 40,000 ft (-304.8 m to 12,192 m)

1.10.6 Shock

All shock specifications assume that the drive is mounted in an approved orientation with the shock input levels measured at the drive mounting screws. The nonoperating specifications assume that the read/write heads are positioned in the shipping zone.

Note. At power-down and during Idle and Standby modes, the read/write heads automatically move to the shipping zone. The head and slider assembly park inside of the maximum data cylinder. When power is applied, the heads recalibrate to track 0.

1.10.6.1 Operating shock

The maximum shock the ST9100A can experience during operation without incurring nonrecoverable data errors is 10 Gs (based on half sine-wave shock pulses of 11 msec).

1.10.6.2 Nonoperating shock

The maximum shock the ST9100A can experience without incurring drive damage or degradation in performance when the drive is subsequently put into operation is 150 Gs (based on half-sine shock pulses of 11 msec).

1.10.7 Vibration

All vibration specifications assume that the drive is mounted in an approved orientation with the vibration input levels measured at the drive mounting screws. The nonoperating specifications assume that the read/write heads are positioned in the shipping zone.

1.10.7.1 Operating vibration

Maximum vibration without drive damage or degradation in performance:

5–22 Hz	0.020-inch displacement (double amplitude)
22-500 Hz	0.5 G acceleration (peak)
500-22 Hz	0.5 G acceleration (peak)
22-5 Hz	0.020-inch displacement (double amplitude)

1.10.7.2 Nonoperating vibration

Maximum vibration without causing physical damage or degradation in performance when the device is subsequently put into operation:

5–22 Hz	0.162-inch displacement (double amplitude)
22-500 Hz	4 Gs acceleration (peak)
500–22 Hz	4 Gs acceleration (peak)
22-5 Hz	0.162-inch displacement (double amplitude)

1.11 Power specifications

The ST9100A receives DC power (+5V), through pin 41 and pin 42 of the AT interface connector; pin 43 is ground.

1.11.1 Power management modes

Power management is required for low-power, portable computer systems. In most systems, you can control power management through the system setup program. The ST9100A features several power management modes, which are described briefly below:

Active mode. The drive is in Active mode during the read/write and seek operations.

Idle-Ready mode. In Idle-Ready mode, the spindle is up to speed and the heads are on track at the last sector accessed. The drive accepts all commands, and returns to Active mode when disc access is necessary.

Idle mode. At power-on, the drive sets the idle timer to enter Idle mode after 5 seconds of inactivity. You can set the idle timer delay using the system setup utility. In Idle mode, the spindle remains up to speed. The heads are parked and latched away from the data zones for maximum

data safety. The buffer remains enabled, and the drive accepts all commands and returns to Active mode any time disc access is necessary.

Standby mode. The drive enters Standby mode when the host sends a Standby Immediate command. The drive can also enter Standby mode after a specifiable length of time has elapsed with the drive in Idle mode. The standby timer delay is system dependent, and is usually established using the system setup utility. In Standby mode, the buffer remains enabled, the heads are parked and the spindle is at rest. The drive accepts all commands, and returns to Active mode any time disc access is necessary.

Sleep mode. The drive enters Sleep mode when a Sleep Immediate command has been received from the host. The heads are parked and the spindle is at rest. The drive leaves Sleep mode when a Hard Reset or Soft Reset command is sent from the host. After a soft reset has been received, the drive exits Sleep mode and enters Standby mode with all current emulation and translation parameters intact.

Rest mode. Some host systems reduce drive power consumption by removing all power from the drive, using a state known as Rest mode. In entering Rest mode, the host saves drive state information (including current logical geometry, set feature parameters, cache status and task file registers) prior to powering down the drive, then restores the drive to its prerest condition once power is restored. Rest mode is implemented using three commands: Rest, Read Drive State, and Restore Drive State. The Rest command prepares the drive for a subsequent Read Drive State command. The Read Drive State command captures the state of the I/O registers and transfers this data to nonvolatile memory within the host. The Restore Drive State command reads the drive state data from memory and restores the drive state based on these data.

Idle and standby timers. The drive sets default time delays for both the idle timer and the standby timer at power-on. In most systems, you can set these delays using the system setup utility. Each time the drive performs an Active function (read, write or seek), the idle timer is reinitialized, and begins the countdown from the specified delay time to zero. If the idle timer reaches zero before any drive activity is required, the drive makes a transition to Idle mode. After making the transition to Idle mode, the drive begins the standby timer countdown. If the standby timer reaches zero before any drive activity is required, the drive makes a transition to Standby mode. In both Idle and Standby mode, the drive accepts all commands, and returns to Active mode when disc access is necessary.

1.11.2 Power consumption

Power requirements for the ST9100A are listed below. All typical measurements are taken at 5V and zero ripple on a 10 MHz AT system. Maximums are measured at 5.25V.

Typical Active mode current and power specifications assume nominal voltages applied, 25°C ambient temperature at sea level, with the spindle rotating (two spindle rotations between each operation) and the drive in default logical geometry. Maximum seek currents and power usage are measured on repetitive one-third-stroke buffered seeks with one-half spindle rotation between each seek. Maximum read/write currents and power are measured with one-half spindle rotation between each operation. Transient state changes may cause current peaks above the maximum levels.

Drive / Mode	Watts RMS (Typical)	Watts RMS (Maximum)	Amps RMS (Maximum)
Spinup	3.5	4.8	0.9
Active: Seeking Read/Write	1.55 1.45	1.65 1.6	0.32 0.30
Idle mode	0.54	0.66	0.12
Standby mode	0.12	0.18	0.027
Sleep mode	0.06	0.11	0.020

1.11.3 Typical current profiles

A typical startup and operation current profile for the ST9100A is shown in Figure 1 on page 8.

1.11.4 Input power noise

Voltage tolerance (including ripple): + 10% - 8%

Maximum permitted input noise ripple is 150 mV (peak-to-peak).

Maximum permitted input noise is 10 MHz.

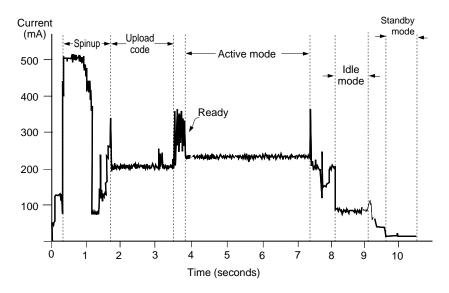


Figure 1. Startup and operation current profile for the ST9100A

1.12 UL/CSA listing

The ST9100A is listed in accordance with UL 1950 and CSA C22.2 (950-M89), and meets all applicable sections of IEC 380, IEC 435, IEC 950, VDE 0806/08.81 and EN 60950 as tested by TUV-Rheinland, North America.

1.13 FCC verification

The ST9100A is intended to be contained solely within a personal computer or similar enclosure (not attached to an external device). As such, the drive is considered to be a subassembly even when it is individually marketed to the customer. As a subassembly, no Federal Communications Commission verification or certification of the device is required.

Seagate Technology, Inc. has tested this device in enclosures as described above to ensure that the total assembly (enclosure, disc drive, motherboard, power supply, etc.) does comply with the limits for a Class B computing device, pursuant to Subpart J, Part 15 of the FCC rules. Operation with noncertified assemblies is likely to result in interference to radio and television reception.

Radio and Television Interference. This equipment generates and uses radio frequency energy and if not installed and used in strict

accordance with the manufacturer's instructions, may cause interference to radio and television reception.

This equipment is designed to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause interference to radio or television, which can be determined by turning the equipment on and off, you are encouraged to try one or more of the following corrective measures:

- · Reorient the receiving antenna.
- Move the device to one side or the other of the radio or TV.
- Move the device farther away from the radio or TV.
- Plug the computer into a different outlet so that the receiver and computer are on different branch outlets.

If necessary you should consult your dealer or an experienced radio/television technician for additional suggestions. You may find helpful the following booklet prepared by the Federal Communications Commission: *How to Identify and Resolve Radio-Television Interference Problems*. This booklet is available from the Superintendent of Documents, U.S. Government Printing Office, Washington, DC 20402. Refer to publication number 004-000-00345-4.

2.0 Drive handling and mounting

2.1 Handling and static-discharge precautions

After unpacking, and prior to system integration, the drive may be exposed to potential handling and ESD hazards. It is mandatory that you observe standard static-discharge precautions. A grounded wrist-strap is preferred.

Handle the drive only by the sides of the head/disc assembly. Avoid contact with the printed circuit board, all electronic components, and the interface connector. Do not apply pressure to the top cover. Always rest the drive on a padded antistatic surface until you mount it in the host system.

2.2 Mounting the ST9100A

You can mount the ST9100A in any orientation, as long as the drive is securely fastened to a rigid frame using four side-mounting screws or four bottom-mounting screws. Allow a minimum clearance of 0.030 inches (0.762 mm) around the entire perimeter of the drive for cooling airflow.

Figure 2 on page 12 provides mounting dimensions for the ST9100A. These drives are designed in accordance with industry-standard MCC direct-mounting specifications, and require the use of MCC-compatible connectors in fixed-mounting applications.

Caution. To avoid damaging the drive:

- Use M3X0.5 metric mounting screws only.
- Do not insert mounting screws more than 0.150 inches (3.81 mm) into the mounting holes.
- Do *not* overtighten the screws (maximum torque: 3 inch-lb).

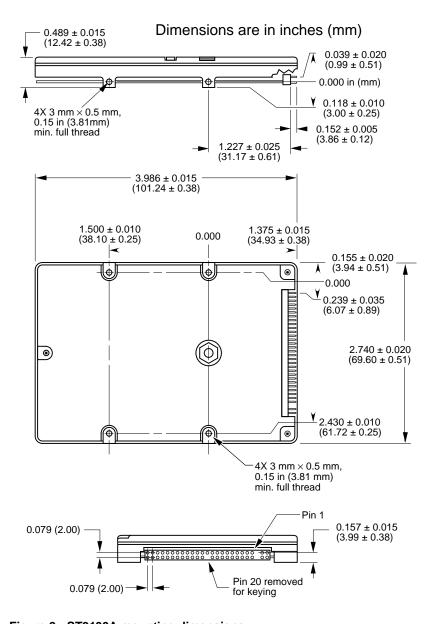


Figure 2. ST9100A mounting dimensions

3.0 AT interface

The ST9100A uses the industry-standard ATA task file interface. The drives support both 8-bit and 16-bit data transfer and have no DMA capability. All data transfers are completed through programmed I/O. Up to two drives can be daisy-chained (as master and slave) on the same host bus.

3.1 Drive configuration

3.1.1 Master/slave selection

A master/slave relationship must be established between drives on the AT bus. Drive 1 is configured as the master and Drive 2 is configured as the slave. Refer to the table below and Figure 3 on page 14 for jumper settings used to configure the drive as a master or a slave.

Jumper for pins A and B	Jumper for pins C and D	Configuration
Removed	Removed	Drive is master; no slave drive present
Removed	Installed	Drive is master; Seagate slave drive present
Installed	Removed	Drive is slave; Seagate master drive present
Installed	Installed	Reserved configuration (do not use)

3.1.2 Remote LED

The drive indicates activity to the host through the DASP— line (pin 39) on the AT interface. This line can be connected to a drive status indicator driving an LED at 5V. The line has a 30 mA nominal current limit.

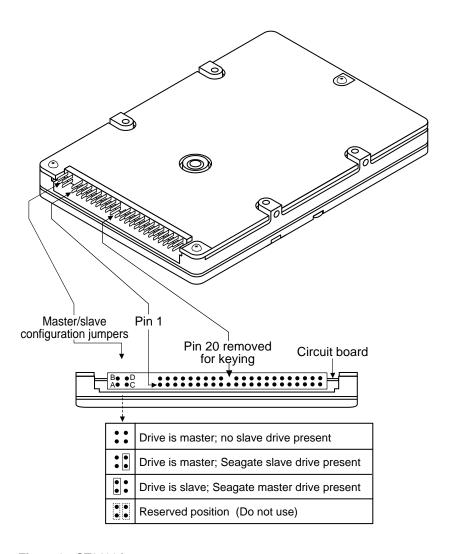


Figure 3. ST9100A connector setup

3.2 Onboard drive diagnostics

At power-on, the drive executes a series of diagnostic tests. A series of LED flashes on the system panel indicate a failure.

Error codes (LED Flashes)	Error type
1	Microprocessor error
2	ROM checksum error
3	AT interface chip failure
5	External RAM error
6	Buffer RAM error

3.3 AT bus signal levels

Signals driven by the drive must have the following output characteristics at the drive connector:

Logic Low	0.0V to 0.4V
Logic High	2.5V to 5.25V

Signals received by the drive must have the following input characteristics, measured at the drive connector:

Logic Low	0.0V to 0.8V
Logic High	2.0V to 5.25V

3.4 AT interface connector

The drive connector is a 44-conductor connector with 2 rows of 22 male pins on 0.079 inch (2 mm) centers (see Figure 4 on page 16).

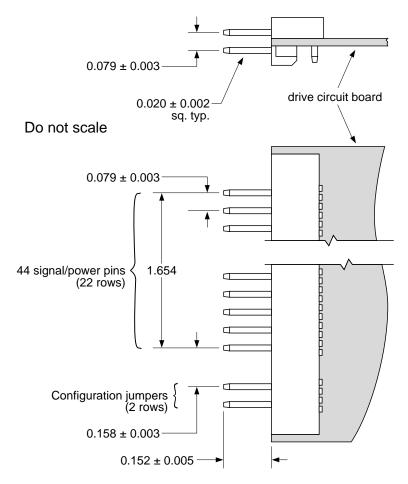
The mating-cable connector is a 44-conductor nonshielded connector with 2 rows of 22 female contacts on 0.079 inch (2 mm) centers. It is recommended that the connectors be keyed by inserting a plug into the pin 20 location of each interface connector. Strain relief is recommended.

Use MCC-compatible connectors, such as Molex part number 87368-442x, for fixed-mounting applications. For applications involving flexible cables or printed circuit cables (PCCs), use Molex part number 87259-4413 or equivalent to connect the system to the drive. Select a connector that provides adequate clearance for the master/slave configuration

jumpers (if the application requires the use of such jumpers). See Figure 4 for details.

3.5 AT interface cable

Maximum cable length is 18 inches (457 mm). It is recommended that the connectors be keyed by the use of a plug in the pin 20 location of each interface connector.



Note. Tolerances are noncumulative over entire range

Figure 4. AT interface connector dimensions

3.6 AT interface connector pin assignments

The following diagram summarizes the signal pin assignments for the ST9100A AT interface connector.

Drive pin #	Signal name	ļ	Host	pin # and signal description
1	Reset-		1	Host Reset
2	Ground		2	Ground
3	← DD7 —		3	Host Data Bus Bit 7
4	← DD8 —		4	Host Data Bus Bit 8
5	← DD6 —		5	Host Data Bus Bit 6
6	← DD9 —		6	Host Data Bus Bit 9
7	← DD5 —		7	Host Data Bus Bit 5
8	← DD10 —		8	Host Data Bus Bit 10
9	← DD4 —		9	Host Data Bus Bit 4
10	← DD11 —		10	Host Data Bus Bit 11
11	← DD3 —		11	Host Data Bus Bit 3
12	← DD12 —		12	Host Data Bus Bit 12
13	← DD2 —		13	Host Data Bus Bit 2
14	← DD13 —		14	Host Data Bus Bit 13
15	← DD1 —		15	Host Data Bus Bit 1
16	◆ DD14 —		16	Host Data Bus Bit 14
17	← DD0 —		17	Host Data Bus Bit 0
18	◆ DD15		18	Host Data Bus Bit 15
19	Ground		19	Ground
20	(removed)		20	(No Pin)
21	Reserved —		21	Reserved
22	Ground		22	Ground
23	◆ DIOW- —		23	Host I/O Write
24	Ground		24	Ground
25	◆ DIOR- —		25	Host I/O Read
26	Ground		26	Ground
27	——— Reserved —		27	Reserved
28	Reserved —		28	Reserved
29	——— Reserved —		29	Reserved
30	Ground		30	Ground
31	INTRQ		31	Host Interrupt Request
32	——— IOCS16- —		32	Host 16 Bit I/O
33	•—— DA1 —		33	Host Address Bus Bit 1
34	PDIAG		34	Passed Diagnostics
35	← DA0 —		35	Host Address Bus Bit 0
36	◆── DA2 —		36	Host Address Bus Bit 2
37	←		37	Host Chip Select 0
38	CS3FX−		38	Host Chip Select 1
39	DASP		39	Drive Active / Slave Present
40	Ground		40	Ground
41	Power —		41	+5V (logic)
42	Power —		42	+5V (motor)
43	_Ground _		43	Ground for power pins
44	Reserved —		44	Reserved

3.7 AT interface commands for the ST9100A

The following commands are specific to the ST9100A. For a description of any AT interface commands not found in this manual and Seagate's implementation of the AT interface, refer to the *Seagate ATA Interface Specification*, publication number 36111-001.

For maximum compatibility, there may be more than one opcode for some commands. In such instances, all opcodes perform in an equivalent manner and are treated identically by the drive.

In all of the following tables, D/S designates the drive select bit and an "X" designates that the register is not used for the particular command. Notations for special register functions are listed in the command table and explained in the command descriptions.

3.7.1 Standby Immediate (E0H / 94H)

When the drive receives this command, it enters Standby mode immediately. The drive sets BSY, initiates a shutdown sequence, enters Standby mode, clears BSY, and generates an interrupt. If the drive is already in Standby mode when this command is received, it sets BSY, clears BSY and generates an interrupt.

Е0н	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command (1F7 _H)	1	1	1	0	0	0	0	0
Cyl. High (1F5 _H)		×						
Cyl. Low (1F4 _H)				>	<			
Drv. Head (1F6 _H)	1	0	1	D/S		>	×	
Sec. Num. (1F3 _H)				>	<			
Sec. Cnt. (1F2 _H)				>	<			

94 _H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command (1F7 _H)	1	0	0	1	0	1	0	0
Cyl. High (1F5 _H)				>	<			
Cyl. Low (1F4 _H)		Х						
Drv. Head (1F6 _H)	1	0	1	D/S)	K	
Sec. Num. (1F3 _H)				>	<			
Sec. Cnt. (1F2 _H)				```	<			

3.7.2 Idle Immediate (E1_H / 95_H / F8_H)

When the drive receives this command, it sets BSY and enters Idle mode. If the drive is in Standby mode, the spinup routine is executed. If the drive is in either Active or Idle mode, the spindle is already up to speed, and the spinup routine is skipped. Next, the drive clears BSY and generates an interrupt.

E1 _H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command (1F7 _H)	1	1	1	0	0	0	0	1
Cyl. High (1F5 _H))	<			
Cyl. Low (1F4 _H)		X						
Drv. Head (1F6 _H)	1	0	1	D/S		>	×	
Sec. Num. (1F3 _H))	<			
Sec. Cnt. (1F2 _H))	<			

95н	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command (1F7 _H)	1	0	0	1	0	1	0	1
Cyl. High (1F5 _H)				>	<			
Cyl. Low (1F4 _H)				>	<			
Drv. Head (1F6 _H)	1	0	1	D/S)	<	
Sec. Num. (1F3 _H)				>	<			
Sec. Cnt. (1F2 _H)				>	<			

F8 _H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command (1F7 _H)	1	1	1	1	1	0	0	0
Cyl. High (1F5 _H)		X						
Cyl. Low (1F4 _H)		X						
Drv. Head (1F6 _H)	1	0	1	D/S)	K	
Sec. Num. (1F3 _H)				>	<			
Sec. Cnt. (1F2 _H)				>	<			

3.7.3 Standby (E2H / 96H)

When the drive receives this command, it sets BSY and makes a transition to Standby mode. Depending on the value placed in the Sector Count register, the drive either enables or disables the standby timer. The drive then clears BSY and generates an interrupt. Placing a zero value in the Sector Count register disables automatic Standby. Placing a nonzero value in the Sector Count register enables the standby timer to count down in 5-second increments. A value of 12 sets the

standby timer for sixty seconds before the Standby routine is initiated. A value of 13 sets the timer for sixty-five seconds. The minimum amount of time allowed for the standby timer is sixty seconds. Consequently, all values from 1–11 have an equivalent effect to a value of 12 for the standby timer. The delay timer is reinitialized by the drive whenever the drive enters Active mode. If the drive is already in Standby mode, this command has no effect. The default power-on condition for this drive has automatic power-down disabled.

E2 _H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command (1F7 _H)	1	1	1	0	0	0	1	0
Cyl. High (1F5 _H)		X						
Cyl. Low (1F4 _H)		Х						
Drv. Head (1F6 _H)	1	0	1	D/S)	<	
Sec. Num. (1F3 _H)		•		>	<			
Sec. Cnt. (1F2 _H)	5	standby	timer d	lelay (in	5-secc	nd incr	ements)

96н	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command (1F7 _H)	1	0	0	1	0	1	1	0
Cyl. High (1F5н)		X						
Cyl. Low (1F4 _H)		Х						
Drv. Head (1F6н)	1	0	1	D/S		>	<	
Sec. Num. (1F3 _H)		X						
Sec. Cnt. (1F2 _H)	S	standby timer delay (in 5-second increments)						

3.7.4 Idle (E3H / 97H)

When the drive receives this command, it sets BSY, makes a transition to Idle mode, sets the standby timer if necessary, clears BSY and generates an interrupt. The minimum amount of time allowed for the idle timer is sixty seconds. Consequently, all values from 1 to 11 have an equivalent effect to a value of 12 for the standby timer.

E3 _H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command (1F7 _H)	1	1	1	0	0	0	1	1
Cyl. High (1F5 _H)		X						
Cyl. Low (1F4 _H)		X						
Drv. Head (1F6 _H)	1	0	1	D/S)	<	
Sec. Num. (1F3 _H)			•	>	<			
Sec. Cnt. (1F2 _H)	5	standby timer delay (in 5-second increments)						

97 _H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command (1F7 _H)	1	0	0	1	0	1	1	1
Cyl. High (1F5 _H))	<			
Cyl. Low (1F4 _H)		Х						
Drv. Head (1F6 _H)	1	0	1	D/S)	K	
Sec. Num. (1F3 _H))	<			
Sec. Cnt. (1F2 _H)		idle timer delay (in 5-second increments)						

3.7.5 Check Power Mode (E5H / 98H)

This command returns a code for the power mode the drive is currently in or making a transition to. When the drive receives this command, it sets BSY, returns a value representing the current mode through the Sector Count register, clears BSY and generates an interrupt.

The return values are as follows:

 00_H = The drive is in, or entering, Standby mode.

FF_H = The drive is in, or entering, either Idle or Active mode.

Е5н	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command (1F7 _H)	1	1	1	0	0	1	0	1
Cyl. High (1F5 _H)				>	<			
Cyl. Low (1F4 _H)		Х						
Drv. Head (1F6 _H)	1	0	1	D/S)	K	
Sec. Num. (1F3 _H)				>	<			
Sec. Cnt. (1F2 _H)				>	<			

00	D:: 7	D:4 0	D:: 5	D:/ 4	D:4 0	D:4 0	D:/ 4	D:: 0
98 _H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command (1F7 _H)	1	0	0	1	1	0	0	0
Cyl. High (1F5н)				>	<			
Cyl. Low (1F4 _H)		Х						
Drv. Head (1F6 _H)	1	0	1	D/S)	K	
Sec. Num. (1F3 _H)				>	<			
Sec. Cnt. (1F2 _H)		X						

3.7.6 Set Sleep Mode (E6H / 99H)

This command tells the drive to enter Sleep mode immediately. When the drive receives this command, it sets BSY, enters Sleep mode, clears BSY and generates an interrupt. When a soft reset is sent from the host, the drive leaves Sleep mode and makes a transition to Standby mode. After a soft reset has been received, the drive exits Sleep mode and enters Standby mode with all emulation and translation parameters intact. After a hard reset has been received, the drive returns to Active mode.

E6 _H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command (1F7 _H)	1	1	1	0	0	1	1	0
Cyl. High (1F5 _H)		×						
Cyl. Low (1F4 _H)		X						
Drv. Head (1F6 _H)	1	0	1	D/S)	<	
Sec. Num. (1F3 _H)				>	<			
Sec. Cnt. (1F2 _H)				>	<			

98н	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Command (1F7 _H)	1	0	0	1	1	0	0	0	
Cyl. High (1F5 _H)		X							
Cyl. Low (1F4 _H)		Х							
Drv. Head (1F6н)	1	0	1	D/S		>	<		
Sec. Num. (1F3 _H)		X							
Sec. Cnt. (1F2 _H)				>	<				

3.7.7 Identify Drive (ECH)

The drive sends this command to system ROM during the system startup process. ROM clears the BUSY status within 100 nsec from power-on, but does not indicate the DRIVE READY status until after the upload of external RAM is complete. This command can be executed before the DRIVE READY status has been asserted.

ECH	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Command (1F7 _H)	1	1	1	0	1	1	0	0	
Cyl. High (1F5 _H)		X							
Cyl. Low (1F4 _H)		Х							
Drv. Head (1F6н)	1	0	1	D/S)	K		
Sec. Num. (1F3 _H)		X							
Sec. Cnt. (1F2 _H)				>	<				

The Identify Drive command causes 512 bytes (256 words) of information to be returned to the host. When the drive receives this command, it sets BSY, stores the information in the sector buffer, sets DRQ, and generates an interrupt.

The following table summarizes the information transferred through the Identify Drive command. Parameters listed with an "x" are variable. See Section 1 of this manual for default parameter settings for the ST9100A.

Word	Description	Value
0	Configuration information: Bit 10: disc transfer ≤ 10 Mbits/sec Bit 6: fixed drive Bit 4: head switch time > 15 µsec Bit 3: not MFM encoded Bit 1: hard sectored disc	045Ан
1	Number of fixed cylinders (default logical emulation): 748	02EC _H
2	Reserved	0000н
3	Number of heads (default): 14	000E _H
4	Number of unformatted bytes per track: 36,240	8D90 _H
5	Number of unformatted bytes per sector: 584	0248 _H
6	Number of sectors per track (default logical emulation): 16	0010 _H
7–9	Reserved	0000н
10–19	Serial Number: (20 ASCII characters, 0000 _H = none)	ASCII
20	Controller type = dual-ported multisector buffer with caching	0003 _H
21	Buffer size (120 Kbytes)	00F0 _H
22	Number of ECC bytes	0010 _H
23–26	Firmware revision (8 ASCII character string): $xx = ROM \text{ ver.}, ss = RAM \text{ ver.}, tt = RAM \text{ ver.}$	xx.ss.tt
27–46	Drive model number: (40 ASCII characters, padded to end of string)	ST9xxx
47	Read Multiple command supported	0000H
48	Cannot perform double word I/O	0000H
49	Capabilities: DMA not supported	0000H
50	Reserved	0000н

Word	Description	Value
51	Minimum PIO data transfer cycle time	0000 _H
52	Minimum DMA transfer cycle time (not supported)	0000н
53	The fields in translation mode may be valid	0001н
54	Number of cylinders (current emulation mode)	XXXXH
55	Number of heads (current emulation mode)	XXXXH
56	Number of sectors per track (current emulation mode)	XXXXH
57–58	Number of sectors (current emulation mode)	XXXXH
59–127	Reserved	0000н
128–159	Vendor unique	0000н
160–255	Reserved	0000н

3.7.8 Set Features (EFH)

This command controls the implementation of various features supported by the drive. When the drive receives this command, it sets BSY, checks the contents of the Features register, clears BSY, and generates an interrupt. If the value in the register does not represent a feature supported by the drive, the command is aborted. Power-on default has the read look-ahead feature enabled, and 4 bytes of ECC. The acceptable values for the Features register are defined as follows:

- 02_H Enable write cache (default)
- 44_H Sixteen bytes of ECC apply on read long and write long commands
- 55_H Disable read look-ahead (read cache) feature
- 66_H Disable reverting to power-on defaults
- 82_H Disable write cache
- AAH Enable read look-ahead (read cache) feature (default)
- BB_H 4 bytes of ECC apply on read long and write long commands (default)
- CC_H Enable reverting to power-on defaults (default)

At power-on, or after a hardware reset, the default values of the features are as indicated above (except for write cache, which is enabled or disabled at power-on). A software reset also changes the features to default values unless a 66H command has been received.

Bit settings for the Set Features command are shown below.

EFH	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
Command (1F7 _H)	1	1	1	0	1	1	1	1		
Cyl. High (1F5 _H)		X								
Cyl. Low (1F4 _H)		Х								
Drv. Head (1F6 _H)	1	0	1	D/S		2	×			
Sec. Num. (1F3 _H))	<					
Sec. Cnt. (1F2 _H)		Х								
Features (1F1 _H)			Set F	- eature	s paran	neter				

3.7.9 Active Immediate (F9_H)

This command causes the drive to enter Active mode immediately. When the drive receives this command, it sets BSY, makes a transition to Active mode, clears BSY and generates an interrupt.

F9 _H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Command (1F7 _H)	1	1	1	1	1	0	0	1	
Cyl. High (1F5 _H)		X							
Cyl. Low (1F4 _H)		Х							
Drv. Head (1F6 _H)	1	0	1	D/S)	K		
Sec. Num. (1F3 _H)		X							
Sec. Cnt. (1F2 _H)				>	<				

3.7.10 Idle and Set Idle Timer (FAH)

This command enables and disables the automatic Idle feature of the drive. When the drive receives this command, it sets BSY, switches to Idle mode, and enables or disables the idle timer according to the value placed in the Sector Count register. The drive then clears BSY and generates an interrupt.

If the value in the sector count is zero, the idle timer is disabled and the drive does not automatically switch to Idle mode. If the value is not zero, the drive switches to Idle mode after the specified delay time has elapsed.

The delay time is specified in the Sector Count register in 100-msec increments. The delay is reinitialized whenever the drive enters Active mode.

Note. The factory set default for the Idle timer is five seconds.

FAH	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
Command (1F7 _H)	1	1	1	1	1	0	1	0		
Cyl. High (1F5 _H)		X								
Cyl. Low (1F4 _H)		X								
Drv. Head (1F6 _H)	1	0	1	D/S		>	<			
Sec. Num. (1F3 _H)		X								
Sec. Cnt. (1F2 _H)		idle timer delay (in 100-msec increments)								

3.7.11 Active and Set Idle Timer (FBH)

This command enables and disables the automatic Idle feature of the drive. When the drive receives this command, it sets BSY, switches to Active mode, and enables or disables the idle timer according to the value placed in the Sector Count register. The drive then clears BSY and generates an interrupt.

If the value in the Sector Count register is zero, the idle timer is disabled and the drive does not automatically switch to Idle mode. If the value is not zero, the drive switches to Idle mode after the specified delay time has elapsed.

The delay time is specified in the Sector Count register in 100-msec increments. The delay is reinitialized whenever the drive enters Active mode.

Note. The factory-set default for the idle timer is five seconds.

FB _H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Command (1F7 _H)	1	1	1	1	1	0	1	1	
Cyl. High (1F5 _H)		X							
Cyl. Low (1F4 _H)		X							
Drv. Head (1F6 _H)	1	0	1	D/S)	×		
Sec. Num. (1F3 _H)		X							
Sec. Cnt. (1F2 _H)		idle tir	ner dela	ay (in 10	00-mse	c increr	ments)		

3.7.12 Check Idle Mode (FDH)

This command reports whether the drive is currently in or making a transition to Idle or Active mode. When the drive receives this command, it sets BSY, loads the appropriate code information into the Sector Count register, clears BSY and generates an interrupt. The default time delay before the drive enters Idle mode is five seconds.

Depending on what state the drive is in or making a transition to, one of the following values is sent:

 00_{H} = The drive is in, or entering, Idle mode.

FF_H = The drive is in, or entering, Active or Standby mode.

FD _H	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Command (1F7 _H)	1	1	1	1	1	1	0	1	
Cyl. High (1F5 _H)		X							
Cyl. Low (1F4 _H)		Х							
Drv. Head (1F6 _H)	1	0	1	D/S)	K		
Sec. Num. (1F3 _H)		X							
Sec. Cnt. (1F2 _H)				>	<				

3.7.13 Rest/Resume commands

Some host systems reduce overall power consumption by temporarily removing power from the disc drive. The Rest/Resume process allows drive-state information to be saved to disc prior to powering down the drive. Once power is restored, the drive-state information is retrieved and used to return the drive to its prerest condition. The drive-state information is saved in a single 512-byte data block that includes current logical geometry, set feature parameters, cache status and task file registers.

The Rest/Resume process involves three commands: Rest, Read Drive State and Restore Drive State. The drive will not recognize and execute these commands unless the Features register contains the value 0AC_H. Any other value in the Features register causes the drive to reject the command with a command abort error.

Note. The Rest/Resume process does not save the contents of data buffers or caches.

3.7.13.1 Rest (E7_H)

The host prepares the drive for a subsequent Read Drive State command by issuing a Rest command. If two drives (master and slave) are present, the host must issue the Rest and Read Drive State commands to the slave prior to issuing them to the master.

Because the Rest mode can be used in addition to the other power management modes, if the BSY or DRQ bits are set, the host should wait up to 30 seconds for these bits to clear after the completion of any prior command. If either the DRQ or BSY bits are set, the host may use the DASP— signal to determine when to initiate Rest mode. The drive asserts DASP— when a Rest command is received and negate it upon completion of the Rest command. After the Rest command is issued, the host should wait up to 10 seconds for the drive to assert INTRQ.

When the drive receives a Rest command, it captures the state of the I/O registers as they existed upon completion of the previous command, then enters Rest mode. After entering Rest mode, the drive rejects any command other than a Read Drive State command with an aborted command error. The Rest mode can only be cleared by power off or reset.

After issuing the Rest command, the host should poll the Alternate Status register to monitor for completion status without clearing the interrupt flag that may have been set for an application program.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
Command (1F7 _H)	1	1	1	0	0	1	1	1		
Cyl. High (1F5 _H)		X								
Cyl. Low (1F4 _H)		Х								
Drv. Head (1F6 _H)	1	0	1	D/S		>	<			
Sec. Num. (1F3 _H)				>	<					
Sec. Cnt. (1F2 _H)		X								
Features (1F1 _H)				0A	Сн					

3.7.13.2 Read Drive State (E9H)

The Read Drive State command allows the host system to save certain drive parameters to nonvolatile system memory before shutting down power to the drive. The host should only issue this command following a successful Rest command. If any command other than a Read Drive State command follows a Rest command, the Rest command is aborted. If a Read Drive State command follows any command other than a Rest command, the Read Drive State command is aborted.

If the drive receives a Read Drive State command while in Rest mode, it transfers essential drive-state information to disc, where the Restore Drive State command can recover it following power-on.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
Command (1F7 _H)	1	1	1	0	1	0	0	1		
Cyl. High (1F5 _H)		X								
Cyl. Low (1F4 _H)		X								
Drv. Head (1F6 _H)	1	0	1	D/S		>	<			
Sec. Num. (1F3 _H)				>	<					
Sec. Cnt. (1F2 _H)		X								
Features (1F1 _H)				0A	Сн					

3.7.13.3 Restore Drive State (EAH)

This command allows the host system to restore the drive to the state it was in at the time of the power-down in Rest mode. If the host has previously caused a Rest mode, it must ensure that the first command issued to the drive (after the drive powers up and is ready to accept commands) is not one that will interfere with the intended resume operation.

The host should only issue a Restore Drive State command when powering up the drive after a successful Read Drive State command. Otherwise the Restore Drive State command is aborted. When the drive receives a Restore Drive State command, it reads the 256 bytes of drive-state information that were saved with the Read Drive State command. This drive-state information is checked for validity. If there is a problem with the data, the drive hangs busy with the trap code set to F5H in all of the AT interface registers. If bit zero of the last word transferred is 0H (reset to 0), INTRQ is not asserted at the completion of this command. If bit zero of the last word transferred is set to 1, INTRQ is asserted following the command.

After issuing the Restore Drive State command, the host should poll the Alternate Status register to monitor for completion status without clearing any interrupt flag that may have been set for an application program.

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0			
Command (1F7 _H)	1	1	1	0	1	0	1	0			
Cyl. High (1F5 _H)		X									
Cyl. Low (1F4 _H)		X									
Drv. Head (1F6 _H)	1	0	1	D/S)	X				
Sec. Num. (1F3 _H)				>	<						
Sec. Cnt. (1F2 _H)		х									
Features (1F1 _H)				0A	Сн						



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